

# ISMVL-2012

## IEEE 42<sup>nd</sup> International Symposium on Multiple-Valued Logic

### FINAL PROGRAM

All events are at the Harbour Towers Hotel & Suites, 345 Quebec Street, Victoria BC, Canada

#### Sunday, May 13, 2012

9:00am	<b>Post-Binary ULSI Workshop Registration – Mezzanine</b>
9:30am	<b>Post-Binary ULSI Workshop – Salon A</b> Workshop Co-chairs: <i>S. Nagayama and N. Homma</i>
5:30pm	<b>ISMVL Registration and Welcoming Reception - Mezzanine</b>

#### Monday, May 14, 2012

8:00am	<b>ISMVL Registration – Mezzanine</b>	
8:45am	<b>ISMVL Opening Remarks – Salon B</b> General Chair: <i>M. Miller</i> , Program Chair: <i>V. Gaudet</i>	
9:00am	<b>Special Panel Session on Upcoming Advances in MVL – Salon B</b> Organizers: <i>T. Hanyu and M. Natsui</i>	
10:00am	<b>Break - Mezzanine</b>	
	<b>Session A1: Wireline &amp; Clocking</b> <b>Salon A:</b> Chair: <i>C. Winstead</i>	<b>Session B1: SAT</b> <b>Salon B:</b> Chair: <i>E. Dubrova</i>
10:20am	Multiple-Valued Time-Based Architecture for Serial Communication Links, <i>M. Rashdan, J. Haslett, and B. Maundy</i>	Building Automated Theorem Provers for Infinitely Valued Logics with Satisfiability Modulo Theory Solvers, <i>C. Ansótegui, M. Bofill, F. Manyà, and M. Villaret</i>
10:45am	Efficient Data Transmission Using Multiple-Valued Pulse-Position Modulation, <i>Y. Yuminaka and M. Okui</i>	Greedy Algorithms, Ordering of Variables, and d-Degenerate Instances, <i>A. Bulatov and C. Wang</i>
11:10am	Systematic Coding Schemes for Low-Power Multiple-Valued Current-Mode Asynchronous Communication Links, <i>A. Matsumoto, N. Onizawa, and T. Hanyu</i>	Extremely Complex 4-Colored Rectangle-Free Grids: Solution of Open Multiple-Valued Problems <i>B. Steinbach and C. Posthoff</i>
11:35am	Global Multiple-Valued Clock Approach for High-Performance Multi-Phase Clock Integrated Circuits, <i>M. Thornton and R. Menon</i>	Using Formal Verification and Robotic Evolution Techniques to Find Contradictions in Laws, <i>T. Sun, L. Sun, and M. Perkowski</i>
12:00pm	<b>Lunch and Symposium Subcommittee Meeting – West Harbour Ballroom</b>	
	<b>Session A2: Quantum Circuits</b> <b>Salon A:</b> Chair: <i>G. Dueck</i>	<b>Session B2: Algebra and Logic</b> <b>Salon B:</b> Chair: <i>H. Machida</i>
1:20pm	Synthesis of Permutative Quantum Circuits with Toffoli and TISC Gates, <i>E. Tsai and M. Perkowski</i>	Two New Classification Theorems on Residuated Monoids, <i>S. Jenei and F. Montagna</i>
1:45pm	ESOP-Inspired Synthesis Method for Ternary Permutative Quantum Circuits with 1-Reduced Post Literals, <i>S. Dhawan and M. Perkowski</i>	Non-Deterministic Matrices for Semi-Canonical Deduction Systems, <i>O. Lahav</i>
2:10pm	Using Hasse Diagrams to Synthesize Ternary Quantum Circuits, <i>M. Hawash and M. Perkowski</i>	Modal Operators on Non-Commutative Residuated Lattices, <i>M. Kondo and M. Kawaguchi</i>
2:35pm	Exact Synthesis of Toffoli Gate Circuits with Negative Control Lines, <i>R. Wille, M. Soeken, N. Przigoda, and R. Drechsler</i>	Prime Filters on Residuated Lattices, <i>M. Kondo and E. Turunen</i>
3:00pm	<b>Break – Mezzanine</b>	



	<b>Session A3: Arithmetic Circuits</b> <b>Salon A:</b> Chair: <i>R. Wille</i>	<b>Session B3: Decision Diagrams</b> <b>Salon B:</b> Chair: <i>F. Manyà</i>
3:25pm	Asynchronous Stochastic Decoding of Low-Density Parity-Check Codes, <i>N. Onizawa, V. Gaudet, T. Hanyu, and W. Gross</i>	Analysis of Multi-State Systems with Multi-State Components Using EVMDDs, <i>S. Nagayama, T. Sasao, and J. Butler</i>
3:50pm	Quaternary 1T-2MTJ Cell Circuit for a High-Density and High-Throughput Nonvolatile Bit-Serial CAM, <i>S. Matsunaga and T. Hanyu</i>	A BDD-Based Approach to Constructing LFSRs for Parallel CRC Encoding, <i>E. Dubrova and S. Mansouri</i>
4:15pm	Unified Current-Source Control for Low-Power Current-Mode Logic Bit-Serial Circuits, <i>S. Kisara and M. Kameyama</i>	Remarks on Shapes of Decision Diagrams and Classes of Multiple-Valued Functions, <i>S. Stanković, R. S. Stanković, and J. T. Astola</i>
4:40pm	Formal Design of Multiple-Valued Arithmetic Algorithms over Galois Fields and its Application to Cryptographic Processors, <i>N. Homma, K. Saito, and T. Aoki</i>	Representation of Incompletely Specified Binary and Multiple-Valued Logic Functions by Compact Decision Diagrams. <i>M. Stanković, S. Stojković, and R. S. Stanković</i>
5:05pm	Complexity Study of Continuous-Valued Number System Adders, <i>B. Zamanlooy, A. Novak, and M. Mirhassani</i>	Multi-Terminal Multiple-Valued Decision Diagrams for Characteristic Function Representing Cluster Decomposition, <i>H. Nakahara, T. Sasao, and M. Matsuura</i>
5:40pm	<b>Excursion – Meet in hotel lobby – the excursion is outdoors, please dress accordingly – partners are welcome</b>	

**Tuesday, May 15, 2012**

9:00am	<b>Invited Address – Salon B</b> <b>Quantum Computing, Cryptography, and Compilers</b> <i>Michele Mosca</i> , University of Waterloo and Perimeter Institute for Theoretical Physics (Canada)	
10:00am	<b>Break – Mezzanine</b>	
	<b>Session C1: Quantum Circuits</b> <b>Salon A:</b> Chair: <i>V. Gaudet</i>	<b>Session D1: Switching Theory</b> <b>Salon B:</b> Chair: <i>C. Moraga</i>
10:20am	Linear Reversible Circuit Synthesis in the Linear Nearest-Neighbor Model, <i>B. Schaeffer and M. Perkowski</i>	Several Remarks on Index Generation Functions, <i>D. Simovici, M. Zimand and D. Pletea</i>
10:45am	Optimal Quantum Circuits of 3-qubits, <i>M. M. Rahman and G. Dueck</i>	Multiple-Valued Input Index Generation Functions: Optimization by Linear Transformation, <i>T. Sasao</i>
11:10am	The Roots of the NOT Gate, <i>A. De Vos and S. De Baerdemacker</i>	Gröbner Bases over Cyclic Post Algebras, <i>B. F. López Martinolich</i>
11:35am	Optimizing the Mapping of Reversible Circuits to Four-Valued Quantum Gate Circuits, <i>M. Soeken, Z. Sasanian, R. Wille, M. Miller, and R. Drechsler</i>	
12:00pm	<b>Lunch and Executive Subcommittee Meeting – West Harbour Ballroom</b>	
	<b>Session C2: Mixed-Signal Design</b> <b>Salon A:</b> Chair: <i>Y. Yuminaka</i>	<b>Session D2: Exploring New Roads</b> <b>Salon B:</b> Chair: <i>B. Steinbach</i>
1:20pm	Energy Efficiency of Multi-bit $\Delta\Sigma$ Modulators Using Inverter-Based Integrators, <i>H. Kotani, R. Yaguchi, and T. Waho</i>	Mosaics, Fermat, Walsh (Aller guten Dinge sind drei), <i>C. Moraga</i>
1:45pm	Current-Source-Sharing Differential-Pair Circuits for a Low Power Fine-Grain Reconfigurable VLSI Architecture, <i>X. Bai and M. Kameyama</i>	SIFAR: Self-Identification of Lags of an Autoregressive TSK-Based Model, <i>A. Veloz, H. Allende-Cid, H. Allende, and R. Salas</i>
2:10pm	Process-Variation-Resilient OTA Using MTJ-Based Multi-Level Resistance Control, <i>M. Natsui, T. Nagashima, and T. Hanyu</i>	Probabilistic Logic Programming with Well-Founded Negation, <i>S. Hadjichristodoulou and D. Warren</i>
2:35pm	<b>Break – Mezzanine</b>	

	<b>Session C3: Biomedical/Sensors</b> <b>Salon A:</b> Chair: <i>T. Hanyu</i>	<b>Session D3: Clones</b> <b>Salon B:</b> Chair: <i>L. Haddad</i>
3:00pm	Issues in Multiple-Valued Multi-Modal Sensor Fusion < <i>M. Janidarmian, Z. Zilic, and K. Radecka</i>	Clones of Incompletely Specified Operations, <i>J. Colic, H. Machida and J. Pantović</i>
3:25pm	Modeling Medical System Threats with Conditional Probabilities Using Multiple-Valued Logic Decision Diagrams, <i>T. Manikas, D. Feinstein, and M. Thornton</i>	Hierarchies of Local Monotonocities and Lattice Derivatives for Boolean and Pseudo-Boolean Functions, <i>M. Couceiro, J.-L. Marichal, and T. Waldhauser</i>
3:50pm	A Fault-Tolerant Area-Efficient Current-Mode ADC for Multiple-Valued Neural Networks, <i>F. Saffar, M. Mirhassani, and M. Ahmadi</i>	GAP vs. PAG, <i>M. Couceiro, E. Lehtonen, and T. Waldhauser</i>
4:15pm	<b>Plenary Session – Salon B</b> MVL Technical Committee Chair: <i>E. Dubrova</i>	
6:30pm	<b>Reception (cash bar) – West Harbour Ballroom</b>	
7:00 pm	<b>Banquet – West Harbour Ballroom</b>	

### Wednesday, May 16, 2012

	<b>Session E1:</b> <b>Quantum Circuits</b> <b>Salon A:</b> Chair: <i>M. Miller</i>	<b>Session F1:</b> <b>Special Session to Honour Ivo G. Rosenberg</b> <b>Salon B:</b> Chair: <i>J. Pantović</i>
8:35am	Banzhaf Index and Boolean Difference, <i>Y. Yamamoto</i>	
9:00am	A Synthesis Flow for Sequential Reversible Circuits, <i>M. Soeken, R. Wille, C. Otterstedt, and R. Drechsler</i>	Centralizing Monoids on a Three-Element Set, <i>H. Machida and I. G. Rosenberg</i>
9:25am	Using the Asynchronous Paradigm for Reversible Sequential Circuit Implementation, <i>D. Feinstein and M. Thornton</i>	The Cardinality of the Set of All Clones Containing a Given Minimal Clone, <i>D. Zhuk</i>
9:50am	Quantum Pseudo-Fractional Fourier Transform Using Multiple-Valued Logic, <i>V. Parasa and M. Perkowski</i>	A Survey on Intersections of Maximal Partial Clones of Boolean Partial Functions, <i>M. Couceiro and L. Haddad</i>
10:15am	A New Approach to Online Testing of TGFSOP-based Ternary Toffoli Circuits, <i>N. Nayeem and J. Rice</i>	Semirigid Systems of Equivalence Relations, <i>C. Delhommé, M. Miyakawa, M. Pouzet, I.G.Rosenberg, and H. Tatsumi</i>
10:40am	<b>Break – Mezzanine</b>	
11:00am	<b>Invited Address – Salon B</b> <b>Honouring Ivo G. Rosenberg: His Contributions to ISMVL</b> <i>Hajime Machida</i> , International Christian University (Japan) and <i>Teruo Hikita</i> , Meiji University (Japan)	
12:00pm	<b>Lunch – Mezzanine</b>	
	<b>Session E2: Special Session to Honour Ivo G. Rosenberg</b> <b>Salon B:</b> Chair: <i>D. Simovici</i> , Co-Organizers: <i>L. Haddad, H. Machida and J. Pantović</i>	
1:20pm	A Tribute to Ivo G. Rosenberg <i>Lucien Haddad and Maurice Pouzet</i>	
1:45pm	Counting Predicates, Subset Surjective Functions, and Counting CSPs <i>A. Bulatov and A. Hedayaty</i>	
2:10pm	Triple Representation Theorem for Homogeneous Effect Algebras <i>J. Paseka and J. Niederle</i>	
2:35pm	<b>Break – Mezzanine</b>	
3:00pm	List-Homomorphism Problems on Graphs and Arc Consistency <i>B. Larose and A. Lemaître</i>	
3:25pm	Rosenberg-Type Completeness Criteria for Subclones of Slupecki's Clone <i>A. Szendrei</i>	
3:50pm	On the Generation of (Minimal) Clones Containing Near-Unanimity Operations <i>S. Kerkhoff</i>	

## RELATED EVENTS

### **4th Workshop on Reversible Computation**

July 2-3, 2012, Copenhagen, Denmark

<http://www.reversible-computation.org/2012/cms/>

Registration Date: June 1, 2012

### **10th International Workshop on Boolean Problems**

September 19-21, 2012, Freiberg, Germany

[http://www.informatik.tu-freiberg.de/prof2/ws\\_bp10/](http://www.informatik.tu-freiberg.de/prof2/ws_bp10/)

Submission Due Date: May 26, 2012

### **22nd International Workshop on Post-Binary ULSI Systems**

May 21, 2013, Toyama, Japan

### **IEEE 43rd International Symposium on Multiple-Valued Logic: ISMVL-2013**

May 21-24, 2013, Toyama, Japan

<http://mvl.jpn.org/ISMVL2013/>

Submission Due Date: November 1, 2012

### **Reed-Muller 2013 Workshop, May 24-25, 2013**

May 24-25 (Sat-Sun), 2013, Toyama Japan

<http://www.lsi-cad.com/RM/>

Submission Due Date: February 1, 2013