ISMVL-2012

IEEE 42nd International Symposium on Multiple-Valued Logic

FINAL PROGRAM

All events are at the Harbour Towers Hotel & Suites, 345 Quebec Street, Victoria BC, Canada

Sunday, May 13, 2012

9:00am	**Post-Binary ULSI Workshop Registration – Mezzanine**
9:30am	**Post-Binary ULSI Workshop – Salon A** Workshop Co-chairs: *S. Nagayama and N. Homma*
5:30pm	**ISMVL Registration and Welcoming Reception - Mezzanine**

Monday, May 14, 2012

8:00am	**ISMVL Registration – Mezzanine**	
8:45am	**ISMVL Opening Remarks – Salon B** General Chair: *M. Miller*, Program Chair: *V. Gaudet*	
9:00am	**Special Panel Session on Upcoming Advances in MVL – Salon B** Organizers: *T. Hanyu and M. Natsui*	
10:00am	**Break - Mezzanine**	
	Session A1: Wireline & Clocking **Salon A:** Chair: *C. Winstead*	**Session B1: SAT** **Salon B:** Chair: *E. Dubrova*
10:20am	Multiple-Valued Time-Based Architecture for Serial Communication Links, *M. Rashdan, J. Haslett, and B. Maundy*	Building Automated Theorem Provers for Infinitely Valued Logics with Satisfiability Modulo Theory Solvers, *C. Ansótegui, M. Bofill, F. Manyà, and M. Villaret*
10:45am	Efficient Data Transmission Using Multiple-Valued Pulse-Position Modulation, *Y. Yuminaka and M. Okui*	Greedy Algorithms, Ordering of Variables, and d-Degenerate Instances, *A. Bulatov and C. Wang*
11:10am	Systematic Coding Schemes for Low-Power Multiple-Valued Current-Mode Asynchronous Communication Links, *A. Matsumoto, N. Onizawa, and T. Hanyu*	Extremely Complex 4-Colored Rectangle-Free Grids: Solution of Open Multiple-Valued Problems *B. Steinbach and C. Posthoff*
11:35am	Global Multiple-Valued Clock Approach for High-Performance Multi-Phase Clock Integrated Circuits, *M. Thornton and R. Menon*	Using Formal Verification and Robotic Evolution Techniques to Find Contradictions in Laws, *T. Sun, L. Sun, and M. Perkowski*
12:00pm	**Lunch and Symposium Subcommittee Meeting – West Harbour Ballroom**	
	Session A2: Quantum Circuits **Salon A:** Chair: *G. Dueck*	**Session B2: Algebra and Logic** **Salon B:** Chair: *H. Machida*
1:20pm	Synthesis of Permutative Quantum Circuits with Toffoli and TISC Gates, *E. Tsai and M. Perkowski*	Two New Classification Theorems on Residuated Monoids, *S. Jenei and F. Montagna*
1:45pm	ESOP-Inspired Synthesis Method for Ternary Permutative Quantum Circuits with 1-Reduced Post Literals, *S. Dhawan and M. Perkowski*	Non-Deterministic Matrices for Semi-Canonical Deduction Systems, *O. Lahav*
2:10pm	Using Hasse Diagrams to Synthesize Ternary Quantum Circuits, *M. Hawash and M. Perkowski*	Modal Operators on Non-Commutative Residuated Lattices, *M. Kondo and M. Kawaguchi*
2:35pm	Exact Synthesis of Toffoli Gate Circuits with Negative Control Lines, *R. Wille, M. Soeken, N. Przigoda, and R. Drechsler*	Prime Filters on Residuated Lattices, *M. Kondo and E. Turunen*
3:00pm	**Break – Mezzanine**	

	Session A3: Arithmetic Circuits **Salon A:** Chair: *R. Wille*	**Session B3: Decision Diagrams** **Salon B:** Chair: *F. Manyà*
3:25pm	Asynchronous Stochastic Decoding of Low-Density Parity-Check Codes, *N. Onizawa, V. Gaudet, T. Hanyu, and W. Gross*	Analysis of Multi-State Systems with Multi-State Components Using EVMDDs, *S. Nagayama, T. Sasao, and J. Butler*
3:50pm	Quaternary 1T-2MTJ Cell Circuit for a High-Density and High-Throughput Nonvolatile Bit-Serial CAM, *S. Matsunaga and T. Hanyu*	A BDD-Based Approach to Constructing LFSRs for Parallel CRC Encoding, *E. Dubrova and S. Mansouri*
4:15pm	Unified Current-Source Control for Low-Power Current-Mode Logic Bit-Serial Circuits , *S. Kisara and M. Kameyama*	Remarks on Shapes of Decision Diagrams and Classes of Multiple-Valued Functions, *S. Stanković, R. S. Stanković, and J. T. Astola*
4:40pm	Formal Design of Multiple-Valued Arithmetic Algorithms over Galois Fields and its Application to Cryptographic Processors, *N. Homma, K. Saito, and T. Aoki*	Representation of Incompletely Specified Binary and Multiple-Valued Logic Functions by Compact Decision Diagrams. *M. Stanković, S. Stojković, and R. S. Stanković*
5:05pm	Complexity Study of Continuous-Valued Number System Adders, *B. Zamanlooy, A. Novak, and M. Mirhassani*	Multi-Terminal Multiple-Valued Decision Diagrams for Characteristic Function Representing Cluster Decomposition, *H. Nakahara, T. Sasao, and M. Matsuura*
5:40pm	**Excursion – Meet in hotel lobby – the excursion is outdoors, please dress accordingly – partners are welcome**	

Tuesday, May 15, 2012

9:00am	**Invited Address – Salon B** ***Quantum Computing, Cryptography, and Compilers*** *Michele Mosca*, University of Waterloo and Perimeter Institute for Theoretical Physics (Canada)	
10:00am	**Break – Mezzanine**	
	Session C1: Quantum Circuits **Salon A:** Chair: *V. Gaudet*	**Session D1: Switching Theory** **Salon B:** Chair: *C. Moraga*
10:20am	Linear Reversible Circuit Synthesis in the Linear Nearest-Neighbor Model, *B. Schaeffer and M. Perkowski*	Several Remarks on Index Generation Functions, *D. Simovici, M. Zimand and D. Pletea*
10:45am	Optimal Quantum Circuits of 3-qubits, *M. M. Rahman and G. Dueck*	Multiple-Valued Input Index Generation Functions: Optimization by Linear Transformation, *T. Sasao*
11:10am	The Roots of the NOT Gate, *A. De Vos and S. De Baerdemacker*	Gröbner Bases over Cyclic Post Algebras, *B. F. López Martinolich*
11:35am	Optimizing the Mapping of Reversible Circuits to Four-Valued Quantum Gate Circuits, *M. Soeken, Z. Sasanian, R. Wille, M. Miller, and R. Drechsler*	
12:00pm	**Lunch and Executive Subcommittee Meeting – West Harbour Ballroom**	
	Session C2: Mixed-Signal Design **Salon A:** Chair: *Y. Yuminaka*	**Session D2: Exploring New Roads** **Salon B:** Chair: *B. Steinbach*
1:20pm	Energy Efficiency of Multi-bit ΔΣ Modulators Using Inverter-Based Integrators< *H. Kotani, R. Yaguchi, and T. Waho*	Mosaics, Fermat, Walsh (Aller guten Dinge sind drei), *C. Moraga*
1:45pm	Current-Source-Sharing Differential-Pair Circuits for a Low Power Fine-Grain Reconfigurable VLSI Architecture< *X. Bai and M. Kameyama*	SIFAR: Self-Identification of Lags of an Autoregressive TSK-Based Model< *A. Veloz, H. Allende-Cid, H. Allende, and R. Salas*
2:10pm	Process-Variation-Resilient OTA Using MTJ-Based Multi-Level Resistance Control, *M. Natsui, T. Nagashima, and T. Hanyu*	Probabilistic Logic Programming with Well-Founded Negation, *S. Hadjichristodoulou and D. Warren*
2:35pm	**Break – Mezzanine**	

	Session C3: Biomedical/Sensors **Salon A:** Chair: *T. Hanyu*	**Session D3: Clones** **Salon B:** Chair: *L. Haddad*
3:00pm	Issues in Multiple-Valued Multi-Modal Sensor Fusion< *M. Janidarmian, Z. Zilic, and K. Radecka*	Clones of Incompletely Specified Operations, *J. Colic, H. Machida and J. Pantović*
3:25pm	Modeling Medical System Threats with Conditional Probabilities Using Multiple-Valued Logic Decision Diagrams, *T. Manikas, D. Feinstein, and M. Thornton*	Hierarchies of Local Monotonicities and Lattice Derivatives for Boolean and Pseudo-Boolean Functions, *M. Couceiro, J.-L. Marichal, and T. Waldhauser*
3:50pm	A Fault-Tolerant Area-Efficient Current-Mode ADC for Multiple-Valued Neural Networks, *F. Saffar, M. Mirhassani, and M. Ahmadi*	GAP vs. PAG, *M. Couceiro, E. Lehtonen, and T. Waldhauser*
4:15pm	**Plenary Session – Salon B** MVL Technical Committee Chair: *E. Dubrova*	
6:30pm	**Reception (cash bar) – West Harbour Ballroom**	
7:00 pm	**Banquet – West Harbour Ballroom**	

Wednesday, May 16, 2012

	Session E1: **Quantum Circuits** **Salon A:** Chair: *M. Miller*	**Session F1:** **Special Session to Honour Ivo G. Rosenberg** **Salon B:** Chair: *J. Pantović*
8:35am	Banzhaf Index and Boolean Difference, *Y. Yamamoto*	
9:00am	A Synthesis Flow for Sequential Reversible Circuits, *M. Soeken, R. Wille, C. Otterstedt, and R. Drechsler*	Centralizing Monoids on a Three-Element Set, *H. Machida and I. G. Rosenberg*
9:25am	Using the Asynchronous Paradigm for Reversible Sequential Circuit Implementation, *D. Feinstein and M. Thornton*	The Cardinality of the Set of All Clones Containing a Given Minimal Clone, *D. Zhuk*
9:50am	Quantum Pseudo-Fractional Fourier Transform Using Multiple-Valued Logic, *V. Parasa and M. Perkowski*	A Survey on Intersections of Maximal Partial Clones of Boolean Partial Functions, *M. Couceiro and L. Haddad*
10:15am	A New Approach to Online Testing of TGFSOP-based Ternary Toffoli Circuits, *N. Nayeem and J. Rice*	Semirigid Systems of Equivalence Relations, *C. Delhommé, M. Miyakawa, M. Pouzet, I.G.Rosenberg, and H. Tatsumi*
10:40am	**Break – Mezzanine**	
11:00am	**Invited Address – Salon B** ***Honouring Ivo G. Rosenberg: His Contributions to ISMVL*** *Hajime Machida,* International Christian University (Japan) and *Teruo Hikita,* Meiji University (Japan)	
12:00pm	**Lunch – Mezzanine**	
	Session E2: Special Session to Honour Ivo G. Rosenberg **Salon B:** Chair: *D. Simovici*, Co-Organizers: *L. Haddad, H. Machida and J. Pantović*	
1:20pm	A Tribute to Ivo G. Rosenberg *Lucien Haddad and Maurice Pouzet*	
1:45pm	Counting Predicates, Subset Surjective Functions, and Counting CSPs *A. Bulatov and A. Hedayaty*	
2:10pm	Triple Representation Theorem for Homogeneous Effect Algebras *J. Paseka and J. Niederle*	
2:35pm	**Break – Mezzanine**	
3:00pm	List-Homomorphism Problems on Graphs and Arc Consistency *B. Larose and A. Lemaître*	
3:25pm	Rosenberg-Type Completeness Criteria for Subclones of Slupecki's Clone *A. Szendrei*	
3:50pm	On the Generation of (Minimal) Clones Containing Near-Unanimity Operations *S. Kerkhoff*	

RELATED EVENTS

4th Workshop on Reversible Computation
July 2-3, 2012, Copenhagen, Denmark
http://www.reversible-computation.org/2012/cms/
Registration Date: June 1, 2012

10th International Workshop on Boolean Problems
September 19-21, 2012, Freiberg, Germany
http://www.informatik.tu-freiberg.de/prof2/ws_bp10/
Submission Due Date: May 26, 2012

22nd International Workshop on Post-Binary ULSI Systems
May 21, 2013, Toyama, Japan

IEEE 43rd International Symposium on Multiple-Valued Logic: ISMVL-2013
May 21-24, 2013, Toyama, Japan
http://mvl.jpn.org/ISMVL2013/
Submission Due Date: November 1, 2012

Reed-Muller 2013 Workshop, May 24-25, 2013Reed-Muller 2013
May 24-25 (Sat-Sun), 2013, Toyama Japan
http://www.lsi-cad.com/RM/
Submission Due Date: February 1, 2013