



**IEEE 42nd International Symposium on Multiple-Valued Logic
ISMVL-2012, Victoria, BC, Canada
PRELIMINARY PROGRAM**

Sunday, May 13, 2012

Time	
9:30am	Post-Binary ULSI Workshop Registration
10:00am	Post-Binary ULSI Workshop Workshop Co-chairs: <i>S. Nagayama and N. Homma</i> (Schedule TBD)
5:30pm	ISMVL Registration and Welcoming Reception

Monday, May 14, 2012

Time		
8:00am	ISMVL Registration	
8:45am	ISMVL Opening Remarks General Chair: <i>M. Miller</i> Program Chair: <i>V. Gaudet</i>	
9:00am	Special Panel Session on Upcoming Advances in MVL Organizers: <i>T. Hanyu and M. Natsui</i>	
10:00am	Break (20 min.)	
	Session A1: Wireline & Clocking Chair: <i>C. Winstead</i>	Session B1: SAT Chair: <i>E. Dubrova</i>
10:20am	[A1.1] Multiple-Valued Time-Based Architecture for Serial Communication Links <i>M. Rashdan, J. Haslett, and B. Maundy</i>	[B1.1] Building Automated Theorem Provers for Infinitely Valued Logics with Satisfiability Modulo Theory Solvers <i>C. Ansotegui, M. Bofill, F. Manyà, and M. Villaret</i>
10:45am	[A1.2] Efficient Data Transmission Using Multiple-Valued Pulse-Position Modulation <i>Y. Yuminaka and M. Okui</i>	[B1.2] Greedy Algorithms, Ordering of Variables, and d-Degenerate Instances <i>A. Bulatov and C. Wang</i>
11:10am	[A1.3] Systematic Coding Schemes for Low-Power Multiple-Valued Current-Mode Asynchronous Communication Links <i>A. Matsumoto, N. Onizawa, and T. Hanyu</i>	[B1.3] Extremely Complex 4-Colored Rectangle-Free Grids: Solution of Open Multiple-Valued Problems <i>B. Steinbach and C. Posthoff</i>
11:35am	[A1.4] Global Multiple-Valued Clock Approach for High-Performance Multi-Phase Clock Integrated Circuits <i>M. Thornton and R. Menon</i>	[B1.4] Using Formal Verification and Robotic Evolution Techniques to Find Contradictions in Laws <i>T. Sun, L. Sun, and M. Perkowski</i>
12:00pm	Lunch and Symposium Subcommittee Meeting (80 min.)	

	Session A2: Quantum Circuits Chair: <i>G. Dueck</i>	Session B2: Algebra and Logic Chair: <i>H. Machida</i>
1:20pm	[A2.1] Synthesis of Permutative Quantum Circuits with Toffoli and TISC Gates <i>E. Tsai and M. Perkowski</i>	[B2.1] Two New Classification Theorems on Residuated Monoids <i>S. Jenei and F. Montagna</i>
1:45pm	[A2.2] ESOP-Inspired Synthesis Method for Ternary Permutative Quantum Circuits with 1-Reduced Post Literals <i>S. Dhawan and M. Perkowski</i>	[B2.2] Non-Deterministic Matrices for Semi-Canonical Deduction Systems <i>O. Lahav</i>
2:10pm	[A2.3] Using Hasse Diagrams to Synthesize Ternary Quantum Circuits <i>M. Hawash and M. Perkowski</i>	[B2.3] Modal Operators on Non-Commutative Residuated Lattices <i>M. Kondo and M. Kawaguchi</i>
2:35pm	[A2.4] Exact Synthesis of Toffoli Gate Circuits with Negative Control Lines <i>R. Wille, M. Soeken, N. Przigoda, and R. Drechsler</i>	[B2.4] Prime Filters on Residuated Lattices <i>M. Kondo and E. Turunen</i>
3:00pm	Break (25 min.)	
	Session A3: Arithmetic Circuits Chair: <i>R. Wille</i>	Session B3: Decision Diagrams Chair: <i>F. Manyà</i>
3:25pm	[A3.1] Asynchronous Stochastic Decoding of Low-Density Parity-Check Codes <i>N. Onizawa, V. Gaudet, T. Hanyu, and W. Gross</i>	[B3.1] Analysis of Multi-State Systems with Multi-State Components Using EVMDDs <i>S. Nagayama, T. Sasao, and J. Butler</i>
3:50pm	[A3.2] Quaternary 1T-2MTJ Cell Circuit for a High-Density and High-Throughput Nonvolatile Bit-Serial CAM <i>S. Matsunaga and T. Hanyu</i>	[B3.2] A BDD-Based Approach to Constructing LFSRs for Parallel CRC Encoding <i>E. Dubrova and S. Mansouri</i>
4:15pm	[A3.3] Unified Current-Source Control for Low-Power Current-Mode Logic Bit-Serial Circuits <i>S. Kisara and M. Kameyama</i>	[B3.3] Remarks on Shapes of Decision Diagrams and Classes of Multiple-Valued Functions <i>S. Stankovic, R. S. Stankovic, and J. T. Astola</i>
4:40pm	[A3.4] Formal Design of Multiple-Valued Arithmetic Algorithms over Galois Fields and its Application to Cryptographic Processors <i>N. Homma, K. Saito, and T. Aoki</i>	[B3.4] Representation of Incompletely Specified Binary and Multiple-Valued Logic Functions by Compact Decision Diagrams <i>M. Stankovic, S. Stojkovic, and R. S. Stankovic</i>
5:05pm	[A3.5] Complexity Study of Continuous-Valued Number System Adders <i>B. Zamanlooy, A. Novak, and M. Mirhassani</i>	[B3.5] Multi-Terminal Multiple-Valued Decision Diagrams for Characteristic Function Representing Cluster Decomposition <i>H. Nakahara, T. Sasao, and M. Matsuura</i>
5:30pm	Excursion	

Tuesday, May 15, 2012

Time		
9:00am	Invited Address: <i>Quantum Computing, Cryptography, and Compilers</i> <i>Michele Mosca</i> , University of Waterloo and Perimeter Institute for Theoretical Physics (Canada)	
10:00am	Break (20 min.)	
	Session C1: Quantum Circuits Chair: <i>V. Gaudet</i>	Session D1: Switching Theory Chair: <i>R. Stankovic</i>
10:20am	[C1.1] Linear Reversible Circuit Synthesis in the Linear Nearest-Neighbor Model <i>B. Schaeffer and M. Perkowski</i>	[D1.1] Several Remarks on Index Generation Functions <i>D. Simovici, M. Zimand and D. Pletea</i>
10:45am	[C1.2] Optimal Quantum Circuits of 3-qubits <i>M. M. Rahman and G. Dueck</i>	[D1.2] Multiple-Valued Input Index Generation Functions: Optimization by Linear Transformation <i>T. Sasao</i>
11:10am	[C1.3] The Roots of the NOT Gate <i>A. De Vos and S. De Baerdemacker</i>	[D1.3] Banzhaf Index and Boolean Difference <i>Y. Yamamoto</i>
11:35am	[C1.4] Optimizing the Mapping of Reversible Circuits to Four-Valued Quantum Gate Circuits <i>M. Soeken, Z. Sasanian, R. Wille, M. Miller, and R. Drechsler</i>	[D1.4] Gröbner Bases over Cyclic Post Algebras <i>B. F. López Martinolich</i>
12:00pm	Lunch and Technical Committee Meeting (80 min.)	
	Session C2: Mixed-Signal Design Chair: <i>Y. Yuminaka</i>	Session D2: Exploring New Roads Chair: <i>B. Steinbach</i>
1:20pm	[C2.1] Energy Efficiency of Multi-bit $\Delta\Sigma$ Modulators Using Inverter-Based Integrators <i>H. Kotani, R. Yaguchi, and T. Waho</i>	[D2.1] Mosaics, Fermat, Walsh (Aller guten Dinge sind drei) <i>C. Moraga</i>
1:45pm	[C2.2] Current-Source-Sharing Differential-Pair Circuits for a Low Power Fine-Grain Reconfigurable VLSI Architecture <i>X. Bai and M. Kameyama</i>	[D2.2] SIFAR: Self-Identification of Lags of an Autoregressive TSK-Based Model <i>A. Veloz, H. Allende-Cid, H. Allende, and R. Salas</i>
2:10pm	[C2.3] Process-Variation-Resilient OTA Using MTJ-Based Multi-Level Resistance Control <i>M. Natsui, T. Nagashima, and T. Hanyu</i>	[D2.3] Probabilistic Logic Programming with Well-Founded Negation <i>S. Hadjichristodoulou and D. Warren</i>
2:35pm	Break (25 min.)	

	Session C3: Biomedical/Sensors Chair: <i>T. Hanyu</i>	Session D3: Clones Chair: <i>L. Haddad</i>
3:00pm	[C3.1] Issues in Multiple-Valued Multi-Modal Sensor Fusion <i>M. Janidarmian, Z. Zilic, and K. Radecka</i>	[D3.1] Clones of Incompletely Specified Operations <i>J. Colic, H. Machida and J. Pantovic</i>
3:25pm	[C3.2] Modeling Medical System Threats with Conditional Probabilities Using Multiple-Valued Logic Decision Diagrams <i>T. Manikas, D. Feinstein, and M. Thornton</i>	[D3.2] Hierarchies of Local Monotonicities and Lattice Derivatives for Boolean and Pseudo-Boolean Functions <i>M. Couceiro, J.-L. Marichal, and T. Waldhauser</i>
3:50pm	[C3.3] A Fault-Tolerant Area-Efficient Current-Mode ADC for Multiple-Valued Neural Networks <i>F. Saffar, M. Mirhassani, and M. Ahmadi</i>	[D3.3] GAP vs. PAG <i>M. Couceiro, E. Lehtonen, and T. Waldhauser</i>
4:15pm	Plenary Session MVL Technical Committee Chair: <i>E. Dubrova</i>	
6:30pm	Banquet	

Wednesday, May 16, 2012

Time		
	Session E1: Special Session to Honour Ivo G. Rosenberg Chair: <i>J. Pantovic</i>	Session F1: Quantum Circuits Chair: <i>M. Miller</i>
9:00am	[E1.1] Centralizing Monoids on a Three-Element Set <i>H. Machida and I. G. Rosenberg</i>	[F1.1] A Synthesis Flow for Sequential Reversible Circuits <i>M. Soeken, R. Wille, C. Otterstedt, and R. Drechsler</i>
9:25am	[E1.2] The Cardinality of the Set of All Clones Containing a Given Minimal Clone <i>D. Zhuk</i>	[F1.2] Using the Asynchronous Paradigm for Reversible Sequential Circuit Implementation <i>D. Feinstein and M. Thornton</i>
9:50am	[E1.3] A Survey on Intersections of Maximal Partial Clones of Boolean Partial Functions <i>M. Couceiro and L. Haddad</i>	[F1.3] Quantum Pseudo-Fractional Fourier Transform Using Multiple-Valued Logic <i>V. Parasa and M. Perkowski</i>
10:15am	[E1.4] Semirigid Systems of Equivalence Relations <i>C. Delhommé, M. Miyakawa, M. Pouzet, I.G.Rosenberg, and H. Tatsumi</i>	[F1.4] A New Approach to Online Testing of TGFSOP-based Ternary Toffoli Circuits <i>N. Nayeem and J. Rice</i>
10:40am	Break (20 min.)	

11:00am	Invited Address: Honouring Ivo G. Rosenberg: His Contributions to ISMVL <i>Hajime Machida</i> , International Christian University (Japan) and <i>Teruo Hikita</i> , Meiji University (Japan)
12:00pm	Lunch (80 min.)
	Session E2: Special Session to Honour Ivo G. Rosenberg Chair: <i>D. Simovici</i> Co-Organizers: <i>L. Haddad, H. Machida and J. Pantovic</i>
1:20pm	A Tribute to Ivo G. Rosenberg <i>Lucien Haddad and Maurice Pouzet</i>
1:45pm	[E2.1] Counting Predicates, Subset Surjective Functions, and Counting CSPs <i>A. Bulatov and A. Hedayaty</i>
2:10pm	[E2.2] Triple Representation Theorem for Homogeneous Effect Algebras <i>J. Paseka and J. Niederle</i>
2:35pm	Break (25 min.)
3:00pm	[E2.3] List-Homomorphism Problems on Graphs and Arc Consistency <i>B. Larose and A. Lemaître</i>
3:25pm	[E2.4] Rosenberg-Type Completeness Criteria for Subclones of Slupecki's Clone <i>A. Szendrei</i>
3:50pm	[E2.5] On the Generation of (Minimal) Clones Containing Near-Unanimity Operations <i>S. Kerkhoff</i>
4:15pm	ISMVL Closing Remarks General Chair: <i>M. Miller</i>